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TITLE: MATRIX PANEL DISPLAY DEVICE

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INVENTOR-INFORMATION:
NAME
KUDO, YASUYUKI
MANO, HIROYUKI
FURUHASHI, TSUTOMU
TSUNEKAWA, SATORU
FUTAMI, TOSHIO
NISHITANI, SHIGEYUKI
OISHI, SUMIHISA
INUZUKA, TATSUHIRO

ASSIGNEE-INFORMATION:

NAME	COUNTRY
HITACHI LTD	N/A
HITACHI VIDEO IND INF SYST INC	N/A

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ABSTRACT:

PURPOSE: To provide a matrix display device which realizes a lower electric power consumption in matrix display devices which display particularly animation images and static images in combination.

CONSTITUTION: The data interface of a data driver 102 is provided with a memory 104 which is provided with two ports for the static images and the moving images, stores the static image data from a CPU 118 and simultaneously outputs the data for one scanning electrode-component, a data latching circuit 103 which latches the moving image data and simultaneously outputs the one scanning electrode-component and a selector means 105 which selects either of both pieces of the output data by a moving image display position signal and outputs the data to a liquid crystal driving circuit. The data interface is provided with a circuit for masking the latch clock of the moving image data at the time of displaying only the static images.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the matrix panel display which is applied to a matrix display, especially indicates a dynamic image and the static image by mixture.
[0002]
[Description of the Prior Art] The conventional liquid crystal display is indicated by the 6th edition of a Hitachi LCD driver LSI data book, and P367 (the Hitachi semiconductor operation division issue). The configuration of the conventional liquid crystal display is explained using drawing 2 . In drawing 2 , 201 shall be a liquid crystal panel and shall be constituted from this example by M dots long and the horizontal N dot. 202 is a data driver represented by Hitachi HD66214, 202a is a data latch circuit and 202b is a liquid crystal drive circuit. 203 is a scan driver represented by Hitachi HD66205, 203a is a shift register circuit and 203b is a liquid crystal drive circuit. Moreover, for liquid crystal display data and 205, as for the Rhine clock and 207, a frame clock and 206 are [204 / a data latch clock and 208] alternating current-ized signals. 209 is a liquid crystal controller represented by Hitachi HD66840, and the indicative data for CRT to which 210 is supplied from a display system, and 211 are synchronizing signal groups supplied from a display system. Furthermore, 212 is a liquid crystal display containing 201-211.
[0003] In the data driver 202, if data latch circuit 202a carries out the sequential latch of the liquid crystal display data 204 with the data latch clock 207 and the liquid crystal display data for 1 scan electrode is incorporated, it will output these to coincidence synchronizing with the fall of the Rhine clock 206. Moreover, liquid crystal drive circuit 202b chooses suitable liquid crystal driver voltage according to the combination of the indicative data from data latch circuit 202a, and the alternating current-ized signal 208, and outputs it to the data electrode of a liquid crystal panel. On the other hand, in the scan driver 203, shift-register-circuit 203a incorporates the "yes" period of the frame clock 205 in the fall of the Rhine clock 206, incorporates it with the Rhine clock 206 after that, and shifts data. Liquid crystal drive circuit 203b chooses suitable liquid crystal driver voltage according to the combination of the data from shift-register-circuit 203a, and the alternating current-ized signal 208, and outputs it to the scan electrode of a liquid crystal panel. Furthermore, the liquid crystal controller 209 generates said indicative data 204 for liquid crystal, and the driver control signal groups 205-208 from the synchronizing signal groups 211 (for example, the VGA mode which is a standard video mode for CRT displays is supported), such as the indicative data 210 for CRT displays, a Vertical Synchronizing signal, and a Horizontal Synchronizing signal. By these actuation, the display image for CRT displays can be displayed on the location for which a liquid crystal panel asks.
[0004] Now, the image information of a different class is displayed on coincidence more often with spread-izing of multimedia in recent years. For example, as shown in drawing 3 , the window of animations, such as animation, may be piled up and displayed into still pictures, such as a text display. The example of a display system configuration of the small information machines and equipment which display such a superposition screen using the liquid crystal display explained previously is shown in

drawing 4 . In drawing 4 401 CPU output data and 403 for CPU and 402 The display controller control signal group for still pictures, 404 still picture memory and 406 for the display controller for still pictures, and 405 Still picture data, 407 is a still picture synchronizing signal group. An animation file and 409 408 An animation display instruction, For the display controller control signal group for animations, and 412, as for animation memory and 414, the display controller for animations and 413 are [410 / animation file output data and 411 / a video data and 415] animation synchronizing signal groups, and 416 is a superposition means. While the display controller for still pictures receives the CPU output data 402 with which 402 is outputted from CPU401, and the display controller control signal group 403 for still pictures and outputs the CPU output data 402 as still picture data 406 for CRT displays through the still picture memory 405, the still picture synchronizing signal group 407 is outputted. On the other hand, the animation file 408 will output the animation file output data 410, if the animation display instruction 409 is received from CPU401. And while, as for 411, the display controller for animations receives the animation file output data 410 and the display controller control signal group 403 for still pictures and outputting the animation file output data 410 as a video data 414 for CRT displays through the animation memory 413, the animation synchronizing signal group 415 is outputted. The still picture data 406, the still picture synchronizing signal group 407 and a video data 414, and the animation synchronizing signal group 415 are sent to the superposition means 416, respectively, and with the superposition means 416, they perform superposition of an animation and a still picture so that an animation may be displayed on the location of the arbitration on the screen specified by CPU. It becomes the configuration that this superposition data is sent to a liquid crystal display 212. Thereby, a liquid crystal display 212 can display the indicative data transmitted on the location for which a liquid crystal panel asks regardless of a dynamic image and a static image.

[0005]

[Problem(s) to be Solved by the Invention] In the system of the conventional small information machines and equipment, since the indicative data sent from CPU will mind two or more memory and data-conversion circuits by the time it is transmitted to a liquid crystal driver as mentioned above, it consumes power in this portion. Moreover, considering the transfer method of an indicative data, the indicative data sent from CPU has transmitted the indicative data to the liquid crystal data driver regardless of change of the contents to being transmitted only when the contents change. Generally, Number Mz and since it is high-speed, this transfer frequency has the large power consumption of the data latch circuit which incorporates this transfer data in a data driver.

[0006] As a method of solving this technical problem, there is a driver with built-in memory represented by Hitachi HD66108. The display system configuration of the small information machines and equipment using this driver with built-in memory is shown in drawing 5 . In drawing 5 , the liquid crystal display with which 501 was equipped with the driver with built-in memory, the liquid crystal data driver in which 502 built memory, and 503 are driver control signal groups by which display memory and 504 are generated by the scan driver, and 505 is generated within a driver.

[0007] In this driver 501 with built-in memory, it is possible for it to be crowded direct picking in the indicative data which display memory 503 has a general-purpose interface, and is sent from CPU401. Moreover, display memory 503 outputs the indicative data for one line to coincidence synchronizing with the fall of the Rhine clock which is one of the driver control signal groups 505 like data latch circuit 202a in the liquid crystal data driver 202 shown in the conventional example. Therefore, memory and a data-conversion circuit until an indicative data is transmitted to a liquid crystal driver become unnecessary to the liquid crystal display system shown in the conventional example, and also in a data driver, incorporation of an indicative data serves as only the time of change of data, and clock frequency also serves as dozens Kz(es). Therefore, the power consumption of a system and a data driver can be reduced.

[0008] However, this method is adapted only about the so-called still picture sent from CPU, and does not support the system which piles up and displays the still picture and animation which were stated in the conventional example. In order to realize this, the display controller for a still picture and animations and a superposition means are needed for the liquid crystal display exterior, and there is a problem on

which system power consumption goes up again.
[0009] The purpose of this invention is offering the liquid crystal driver which can stop the power consumption of a system also in the system which piles up and displays a still picture and an animation as mentioned above.
[0010]
[Means for Solving the Problem] It considers displaying a still picture which is the above-mentioned technical problem, and an animation with superposition and a low power. First, what is necessary is just to build memory in appearance mentioned above in a data driver, in order to stop power consumption of a data driver and a system to a still picture. Next, what is necessary is to input independently two kinds of indicative datas, a still picture and an animation, into a data driver, and just to pile up within a data driver, in order to realize this, without using a superposition means of the exterior used as an increment in power consumption etc. to superposition of a still picture and an animation. Paying attention to this point, a liquid crystal data driver of this invention established a selector means to have stored 2 port **** an object for still pictures, and for animations, and still picture data from CPU for a data interface, to have chosen ********** of memory which outputs data for 1 scan electrode to coincidence, a data latch circuit which latches a video data and is outputted to 1 scan electrode part coincidence, and both output data with an animation display position signal, and to output to a liquid crystal drive circuit. Moreover, when displaying only a still picture, latch actuation of a video data prepared a circuit which carries out the mask of the latch clock of a video data, when displaying only a still picture, in order to consume excessive power.
[0011]
[Function] Since a transfer rate becomes slow while memory and a data-conversion circuit until an indicative data is transmitted to a liquid crystal driver by building in the memory which is crowded direct picking in the indicative data from CPU in a liquid crystal data driver become unnecessary, power consumption decreases. Moreover, it was made to correspond to the superposition display of still picture data and a video data by piling up the data interface of a liquid crystal data driver by 2 port **** the object for still pictures, and for animations, and piling up each data inside. An external superposition means etc. becomes unnecessary by this, and power consumption decreases. Furthermore, since the data latch means for video datas does not operate when there is no animation display instruction, it can stop the power consumption when displaying only a still picture.
[0012]
[Example] Hereafter, the example of this invention is explained using drawing 1 and drawing 6 - drawing 10 .
[0013] Drawing 1 is the block diagram showing the configuration of the liquid crystal data driver of one example of this invention, and a liquid crystal display.
[0014] In drawing 1 , 101 shall be an electrochromatic display panel and shall be constituted from this example by a horizontal N dot, M dots long, and the RGB length stripe. 102 is the data driver of one example of this invention, and, as for a data selector and 106, the still picture display memory in which 103 has a video data latch circuit and an interface with general-purpose 104, and 105 are [a selection data latch circuit and 107] liquid crystal drive circuits. 108 is a scan driver represented with Hitachi HD66214. 109 is a video data, the data clock with which 110 synchronized with the video data 109, and 111 are the Rhine clocks, and the video data for one line is sent one period of the Rhine clock 111. 112 is an alternating current-ized signal and determines the polarity of the voltage impressed to a liquid crystal cell in the state of this signal. 113 is a frame clock and one period of the frame clock 113 is an one-frame period. 114 is an animation display signal and determines the existence of a movie display in the state of this signal. 115 is an animation controller and generates a video data 109, the driver control signals 110-113, and the animation display signal 114. 116 is still picture data, 117 is a memory control signal group, and these are signals which control the writing to the memory built in the data driver 102, and the address. 118 is CPU and outputs still picture data and a memory control signal group. 119 is a data latch clock generation circuit, and generates the data latch clock 120 from a data clock 110 and the animation display signal 114. 121 is the liquid crystal display which used the liquid crystal data driver of

one example of this invention.
[0015] First, actuation of the liquid crystal data driver 102 of one example of this invention is explained using the timing chart shown in drawing 6 .
[0016] If the video data latch circuit 103 carries out the sequential latch of the video data 109 with the data latch clock 120 and the liquid crystal display data for 1 scan electrode is incorporated, it will output these synchronizing with the start of the Rhine clock 111. here, as shown in drawing 6 , including location data 109b for boiling a video data 109 apart from indicative-data 109a, and determining the display position of an animation, the sequential latch also of this location data 109b is carried out with the data latch clock 120, and the location data for 1 scan electrode is outputted synchronizing with the start of the Rhine clock 111. Here, since indicative-data 109a (b1, b5, bN, etc. in drawing 6) which has "0" in location data 109b is data which is not selected, the value is arbitrary and is good.
[0017] On the other hand, the still picture display memory 104 outputs the still picture data for 1 scan electrode synchronizing with the standup of the Rhine clock 111 while storing the still picture data 116 in the address specified by the memory control signal group. A data selector 105 chooses a video data, when location data 109b which is a select signal is "1", it chooses still picture data at the time of "0", and outputs. And the selection data latch circuit 106 latches and outputs the selected indicative data in falling of the Rhine clock 111. The liquid crystal drive circuit 107 chooses suitable liquid crystal driver voltage according to the combination of the indicative data from the selection data latch circuit 106, and the alternating current-ized signal 112, and outputs it to the data electrode of a liquid crystal panel.
[0018] Next, actuation of the data latch clock generation circuit 119 is explained using explanatory drawing of drawing 7 of operation, and the timing chart of drawing 8 . The purpose of the data latch clock generation circuit 119 of operation is to stop the clocked into of the video data latch circuit 103, and prevent useless power consumption, when displaying only a still picture. In order to realize this, the data latch clock generation circuit 119 outputs the condition of a data clock 110 as a data latch clock 120 as it is, when the animation display signal 114 displays "1", i.e., an animation, as shown in drawing 7 , and when not displaying "0", i.e., an animation, it outputs "0." This is easily realizable by taking the AND of the animation display signal 114 and the data latch clock 120. In addition, the animation display signal in this example changes, and timing is taken as the standup and match of the frame clock 113 for simplification. Therefore, the timing chart of the data latch clock generation circuit 119 comes to be shown in drawing 8 .
[0019] What is necessary is to judge animation display in Rhine and just to suspend a transfer of a video data and a data latch clock in Rhine which does not display an animation, in order to attain system low-power-ization further although the display judging of animation display is performed for every frame and the mask of a data latch clock is performed in this example. And it is necessary for the data selector 105 to select the still picture in the meantime. The data latch circuit for for example, location data can realize this actuation, if it is made to be reset by "0" by "yes" of the selector line clock 111 each time. That is, unless a video data and a data latch clock are transmitted, location data 109b which is a select signal is still "0", and a data selector 105 can continue choosing still picture data. In addition, as for the output control of a video data and a data latch clock, it is desirable to carry out by the animation controller.
[0020] Moreover, actuation of a scan driver is the same as that of the conventional scan driver, incorporates the "yes" period of the frame clock 113 in the fall of the Rhine clock 111, incorporates it with the Rhine clock 111 after that, shifts data, chooses suitable liquid crystal driver voltage according to combination with the alternating current-ized signal 112, and outputs it to the scan electrode of a liquid crystal panel.
[0021] The display system configuration of the small information equipment machine which piles up and displays a still picture and an animation becomes like drawing 9 using the liquid crystal display 121 of one example of this invention explained above. First, the still picture data 109 from CPU118 and the memory control signal group 116 are outputted to the direct liquid crystal display 121. On the other hand, the animation file 408 will output the animation file output data 410, if the animation display instruction 409 which specifies a display and location of an animation is received from CPU118. And

the display controller 115 for animations generates a video data 109 and the driver control signal groups 110-113 through animation memory from the animation file output data 410 and the display controller control signal group 403 for animations, and changes the animation display instruction 409 inputted, and generates the animation display signal 114 which is set to "1" with the frame which displays an animation, and is set to "0" with the frame which is not displayed. These signals are outputted to a liquid crystal display 121.

[0022] As explained above, the liquid crystal data driver in one example of this invention has the memory which can carry out direct access of the still picture data from CPU, the data latch circuit which incorporates a video data independently, and the processing section which piles both up. Therefore, external circuits, such as conversion of CPU data and superposition processing, become unnecessary to the system of a superposition display of an animation and a still picture. Therefore, compared with the former, a low power superposition display system is realizable.

[0023] Moreover, the increase of the color number and the given display of an animation portion are realizable by performing gradation processing of FRC, a dither, etc. between a video data and a liquid crystal display, as shown in drawing 10 .

[0024] In addition, one example of this invention cannot be based on the element configuration of a liquid crystal panel, for example, can be applied to STN mold liquid crystal, TFT mold liquid crystal, MIM mold liquid crystal, etc.

[0025] Next, the 2nd example of this invention is shown. The 2nd example of this invention prepares a gradation processing facility in a liquid crystal data driver, and offers the multiple color display screen. Hereafter, the 2nd example of this invention explains the case where use a liquid crystal panel as simple matrix type liquid crystal (for example, STN mold liquid crystal), and it indicates by gradation using a Pulse-Amplitude-Modulation method (it is called a PHM method below), using drawing 11 - drawing 15 .

[0026] This example explains the number of gradation as 4 gradation (2 bits of input gradation data).

[0027] Drawing 11 is the block diagram showing the configuration of the liquid crystal data driver of the 2nd example of this invention. In drawing 11 , 1101 is the data driver of this invention 2nd, and, for the still picture display memory in which 1102 has a video data latch circuit and an interface with general-purpose 1103, and 1104, as for a selection data latch circuit and 1106, a data selector and 1105 are [a PHM circuit and 1107] liquid crystal drive circuits. 1108 is a video data transmitted from an animation controller, and has 2-bit gradation information in this example. 1109 is still picture data transmitted from CPU, and has 2-bit gradation information like a video data. Moreover, 1110 is the supply voltage of 8 level for driving liquid crystal. In addition, the driver control signals 111-114 and the animation display signal 120 are equal to what was shown in the one example of this invention.

[0028] Actuation of the liquid crystal data driver 1101 of the 2nd example of this invention is explained.

[0029] If the video data latch circuit 1102 carries out the sequential latch of the gradation high order data of a video data 1108, low order data, and the location data with the data latch clock 120, respectively and the data for 1 scan electrode is incorporated, it will output these synchronizing with the start of the Rhine clock 111. Moreover, the still picture display memory 1103 has two planes the object for gradation high order data, and for low order data, and it outputs the still picture data for 1 scan electrode synchronizing with the standup of the Rhine clock 111 while it stores the still picture data 116 in the address specified by the memory control signal group. When the location data contained in a video data 1108 is "1", a data selector 1104 chooses still picture data for every low order data with gradation high order data, respectively at the time of "0", and outputs a video data to it. And the selection data latch circuit 1105 latches and outputs the selected indicative data in falling of the Rhine clock 111. The PHM circuit 1106 divides a scan period (Rhine clock period) into two, and in the first half, in the second half, it changes gradation data so that the display low order data corresponding to gradation low order data in the display high order data corresponding to gradation high order data may be outputted. The liquid crystal drive circuit 1107 chooses liquid crystal driver voltage according to the combination of the indicative data outputted from the PHM circuit circuit 1106, and the alternating current-ized signal 112,

and outputs it to the data electrode of a liquid crystal panel.
[0030] Here, the configuration of the PHM circuit 1106 is shown in drawing 12 . For gradation low order data, a 1203 select-signal generation circuit, and 1204, as for an indicative-data generation selector and 1206, in drawing 12 , a select signal and 1205 are [1201 / gradation high order data and 1202 / display high order data and 1207] display low order data. When it becomes "1" by "yes" of the Rhine clock 111 in the one half of the counted value which presetting is carried out, counts the number of the data latch clocks 120 after that, and the counted value counts within a scan period, the select signal generation circuit 1203 operates so that "0" may be outputted. The indicative-data generation selector 1204 chooses gradation high order data, when the select signal 1202 generated in the select signal generation circuit 1201 is "1", it chooses gradation low order data at the time of "0", and outputs this as display low order data 1207. Here, the display high order data 1206 turns into the gradation high order data 1201. That is, a PHM circuit operates so that gradation high order data may be outputted and gradation low order data may be outputted for display high order data and low order data to display high order data to gradation high order data and display low order data in the second half in the first half of a scan period.
[0031] Next, the liquid crystal drive circuit 1107 chooses and outputs one voltage value among voltage levels V0-V7 according to the combination of the indicative datas 1206 and 1207 which set to "1" display ON sent from the PHM circuit 1106, and the alternating current-ized signal 112, as shown in drawing 13 . The relation of voltage levels V0-V7 is V0>V1>V2>V3>V4>V5>V6>V7, as shown in drawing 14 . In addition, the non-choosing scan voltage level of a scan driver is V8, when the alternating current-ized signal 112 is "0" and it is V9 and "1", V9 is the middle level of V5 and V6, and V8 is the middle level of V1 and V2. Moreover, a selection scan voltage level is set to V7, when the alternating current-ized signal 112 is "0" and it is V0 and "1."
[0032] If the function of the PHM circuit 1106 and the liquid crystal drive circuit 1107 is summarized to a timing chart, it will become like drawing 15 and 4 gradation 64 color specification will become possible also about the portion of a still picture.
[0033] As explained above, the liquid crystal data driver in the 2nd example of this invention has the memory which can carry out direct access of the still picture gradation data from CPU, the data latch circuit which incorporates animation gradation data independently, the processing section which piles both up, and the gradation processing section which changes gradation data into a liquid crystal gradation display. Therefore, it is possible to increase the color number of a still picture portion about the liquid crystal display which has a simple matrix panel in addition to the effect of one example of this invention.
[0034] Furthermore, since [which is combined with gradation processing of the exterior shown in drawing 10 about the animation portion etc.] things can be carried out, it is possible to increase the color number further.
[0035] In addition, what is necessary is just to increase the plane of a data latch circuit and memory, and the number of partitions of a scan period and the number of level of selection voltage further, in order to carry out and to perform a multicolor display, the increase of the number of bits, and although the gradation number of bits of this example was made into 2 bits. Moreover, although the gradation art in a liquid crystal driver was made into the PHM method in this example, it was not necessarily restricted to this, for example, pulse width modulation, the aforementioned FRC method, and a dither method may be used.
[0036] In the 2nd example of this invention, the simple matrix type liquid crystal (for example, STN mold liquid crystal) panel was targetted. On the other hand, the 3rd example of this invention shows the liquid crystal data driver which realizes multiple color-ization of a static image in a bitter taste tape matrix type liquid crystal (for example, TFT mold liquid crystal) panel. In addition, the number of gradation is explained as 4 gradation (2 bits of input gradation data) about this example as well as the 2nd example of this invention. Hereafter, the 3rd example of this invention is explained using drawing 16 and drawing 17 . Drawing 16 is the block diagram showing the configuration of the liquid crystal data driver of the 3rd example of this invention. In drawing 16 , 1601 is the data driver of this invention

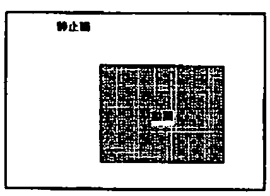
3rd, and it is the supply voltage of 4 level for 1602 to drive a liquid crystal drive circuit and for 1603 drive liquid crystal. Other portions are equal to what was shown in the 2nd example of this example.
[0037] Actuation of the liquid crystal data driver 1601 of the 3rd example of this invention is explained.
[0038] If the video data latch circuit 1102 carries out the sequential latch of the gradation high order data of a video data 1108, low order data, and the location data with the data latch clock 120, respectively and the data for 1 scan electrode is incorporated, it will output these synchronizing with the start of the Rhine clock 111. Moreover, the still picture display memory 1103 has two planes the object for gradation high order data, and for low order data, and it outputs the still picture data for 1 scan electrode synchronizing with the standup of the Rhine clock 111 while it stores the still picture data 116 in the address specified by the memory control signal group. When the location data contained in a video data 1108 is "1", a data selector 1104 chooses still picture data for every low order data with gradation high order data, respectively at the time of "0", and outputs a video data to it. And the selection data latch circuit 1105 latches and outputs the selected indicative data in falling of the Rhine clock 111. The liquid crystal drive circuit 1602 chooses and outputs one voltage value among the liquid crystal driver voltages 1603 of ** 4 level according to the combination of the indicative data outputted from the selection data latch circuit 1105, and the alternating current-ized signal 112, as shown in drawing 17 . The relation of voltage levels V0-V7 is V0>V1>V2>V3>V4.
[0039] As explained above, the liquid crystal data driver in the 3rd example of this invention has the liquid crystal drive circuit which outputs the memory which can carry out direct access of the still picture gradation data from CPU, the data latch circuit which incorporates animation gradation data independently, the processing section which piles both up, and the voltage corresponding to gradation data. Therefore, it is possible to increase the color number of a still picture portion about the liquid crystal display which has an active-matrix panel in addition to the effect of one example of this invention.
[0040] Furthermore, since [which is combined with gradation processing of the exterior shown in drawing 10 about that of an animation portion etc.] things can be carried out, it is possible to increase the color number further.
[0041] In addition, further, although the gradation number of bits of this example was made into 2 bits, the increase of the number of bits, and in order to carry out and to perform a multicolor display, gradation processing of FRC etc. may be built in that what is necessary is just to increase the number of level of a data latch circuit, and the plane of memory and selection voltage.
[0042]
[Effect of the Invention] Since a transfer rate becomes slow while memory and a data-conversion circuit until an indicative data is transmitted to a liquid crystal driver by building in the memory which is crowded direct picking in the indicative data from CPU in a liquid crystal data driver become unnecessary, power consumption decreases compared with the former. Moreover, it can respond to the superposition display of still picture data and a video data by piling up the data interface of a liquid crystal data driver by 2 port **** the object for still pictures, and for animations, and piling up each data inside. An external superposition means etc. becomes unnecessary by this, and power consumption decreases. Furthermore, since the data latch means for video datas does not operate when there is no animation display instruction, it can stop the power consumption when displaying only a still picture. Moreover, the color number of an animation portion can be increased by preparing a gradation processing circuit outside. Furthermore, the color number of a still picture can also be increased by preparing a gradation processing circuit in a liquid crystal data driver.

[Translation done.]

２０８…交流化信号、
２０９…液晶コントローラ、
２１０…ＣＲＴ用表示データ、
２１１…同期信号群、
２１２…液晶表示装置、
４０１…ＣＰＵ、
４０２…ＣＰＵ出力データ、
４０３…静止画用表示コントローラ制御信号群、
４０４…静止画用表示コントローラ、
４０５…静止画メモリ、
４０６…静止画データ、
４０７…静止画同期信号群、
４０８…動画ファイル、
４０９…動画表示命令、
４１０…動画ファイル出力データ、
４１１…動画用表示コントローラ制御信号群、
４１２…動画用表示コントローラ、
４１３…動画メモリ、
４１４…動画データ、
４１５…動画同期信号群、
４１６…重ね合わせ手段、
５０１…液晶表示装置、
５０２…液晶データドライバ、
５０３…表示メモリ、
５０４…走査ドライバ、
５０５…ドライバ制御信号群、
１１０１…データドライバ、
１１０２…動画データラッチ回路、
１１０３…静止画表示メモリ、
１１０４…データセレクタ、
１１０５…セレクトデータラッチ回路、
１１０６…ＰＨＭ回路、
１１０７…液晶駆動回路、
１１０８…動画データ、
１１０９…静止画データ、
１１１０…液晶駆動電源電圧群、
１２０１…階調上位データ、
１２０２…階調下位データ、
１２０３…セレクト信号生成回路、
１２０４…セレクト信号、
１２０５…表示データ生成セレクタ、
１２０６…表示上位データ、
１２０７…表示下位データ、
１６０１…データドライバ、
１６０２…液晶駆動回路、
１６０３…液晶駆動電源電圧群。

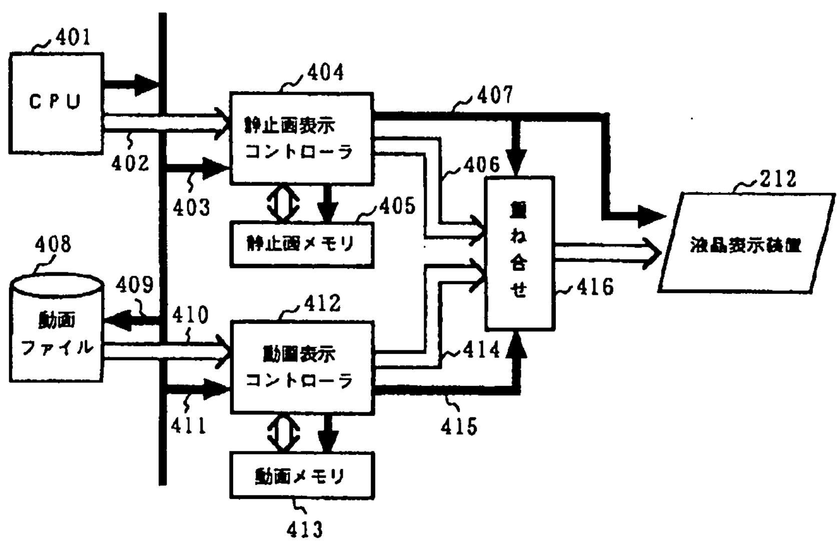
【図３】

図 3



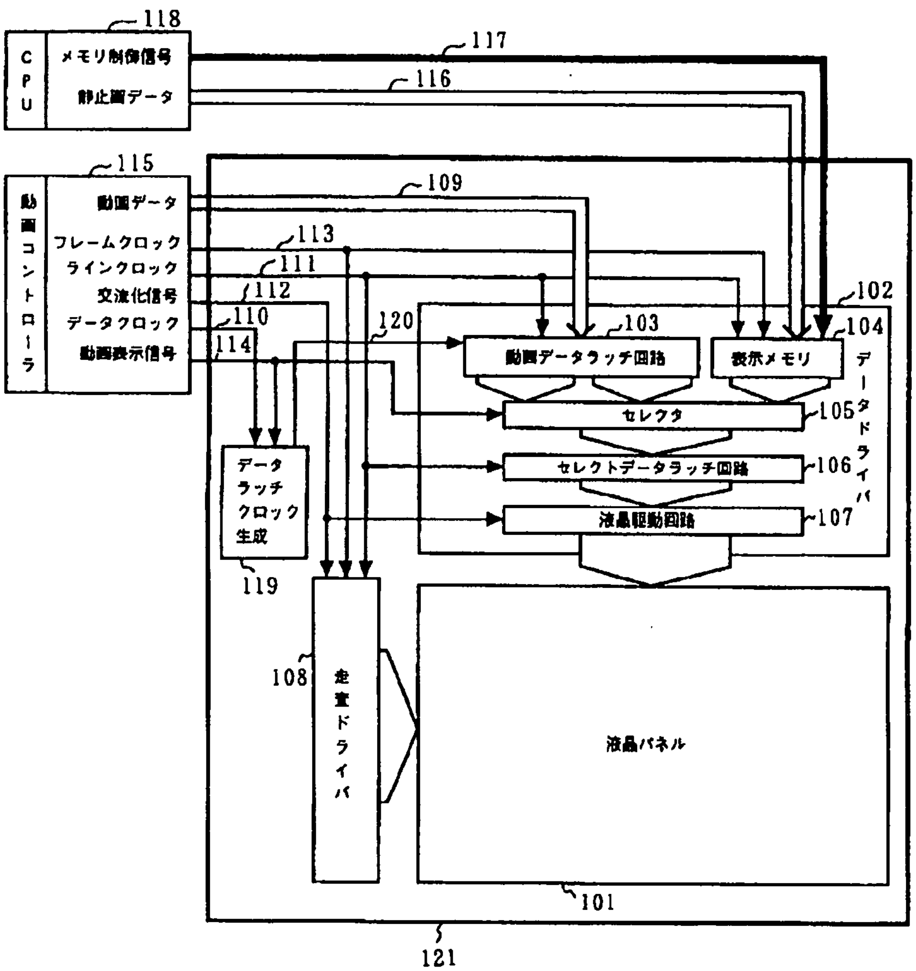
【図４】

図 4



【図1】

図 1



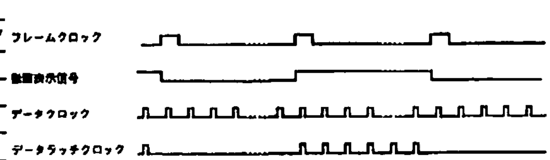
【図7】

図 7

データクロック	動画表示信号	データラッチクロック
0	0	0
1	0	0
0	1	0
1	1	1

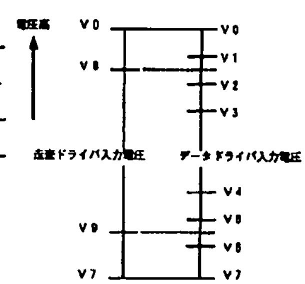
【図8】

図 8



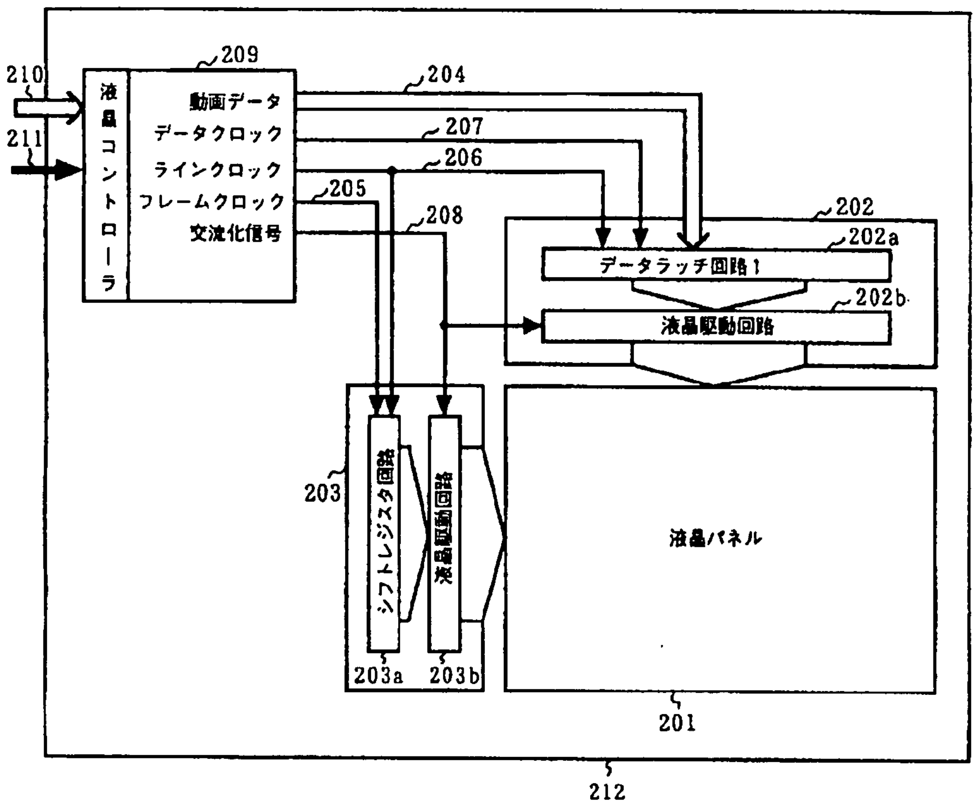
【図14】

図 14



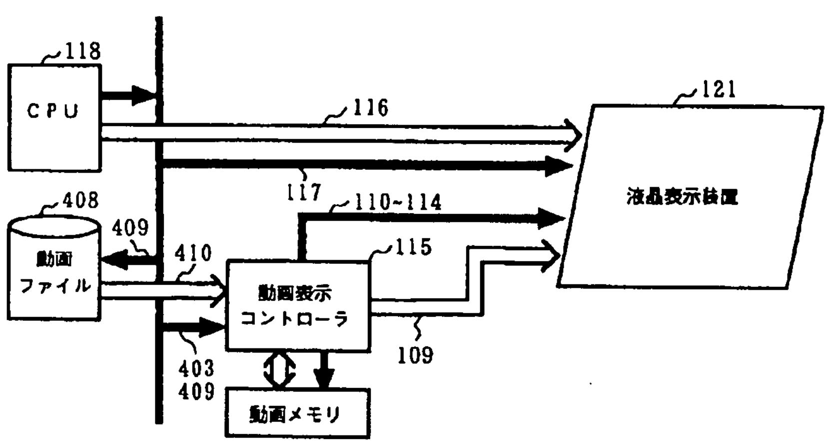
【図2】

図 2



【図9】

図 9



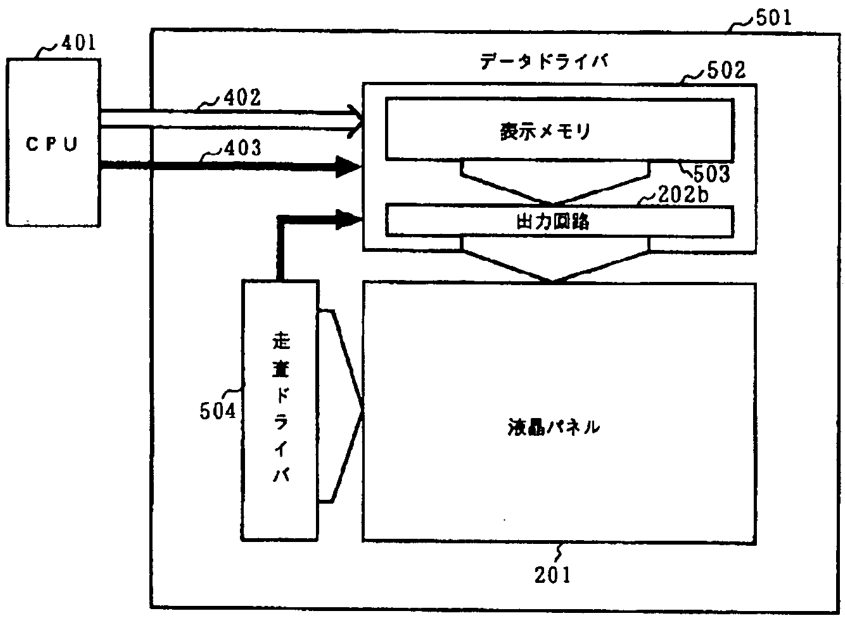
【図13】

図 13

交流化信号	階調上位データ	階調下位データ	出力電圧
0	0	0	V4
	0	1	V5
	1	0	V6
	1	1	V7
1	0	0	V3
	0	1	V2
	1	0	V1
	1	1	V0

【図5】

図 5



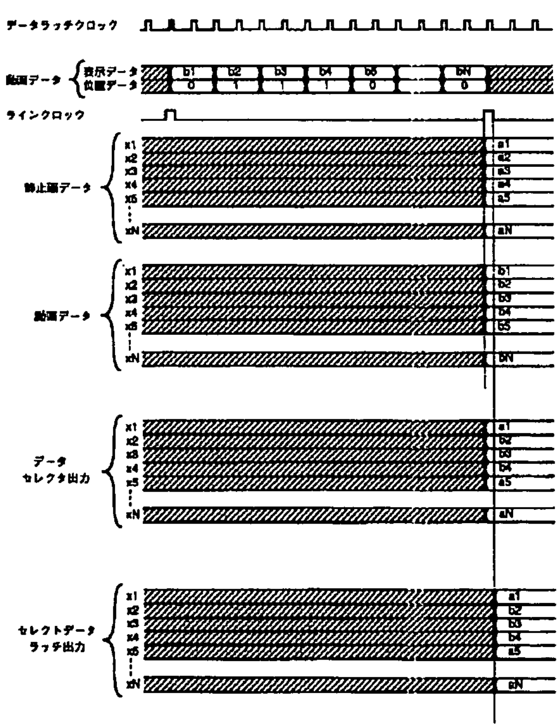
【図17】

図 17

交流化信号	階調上位データ	階調下位データ	出力電圧
0	0	0	V0
	0	1	V1
	1	0	V2
	1	1	V3
1	0	0	V3
	0	1	V2
	1	0	V1
	1	1	V0

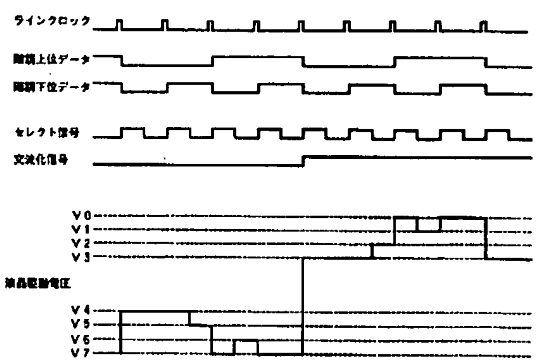
【図6】

図 6



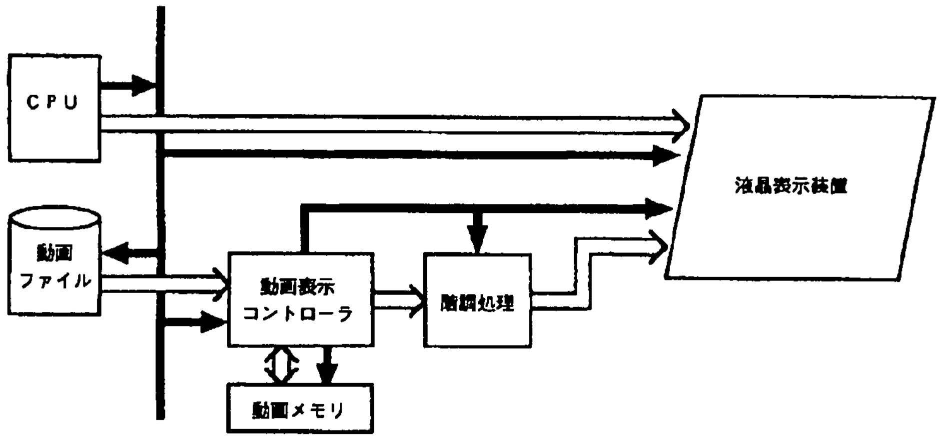
【図15】

図 15



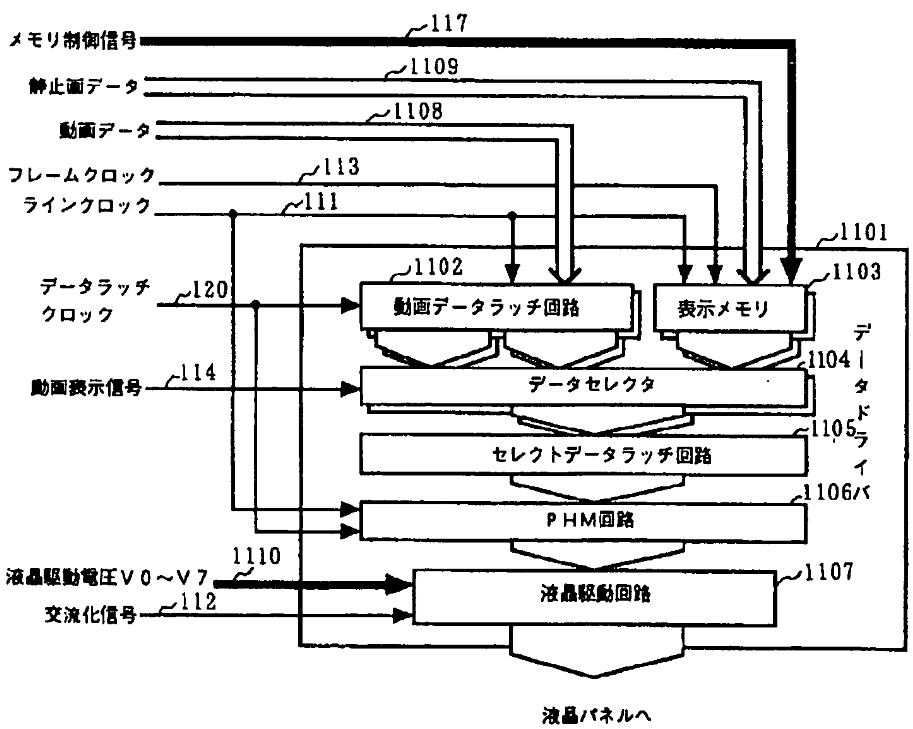
【図10】

図 10

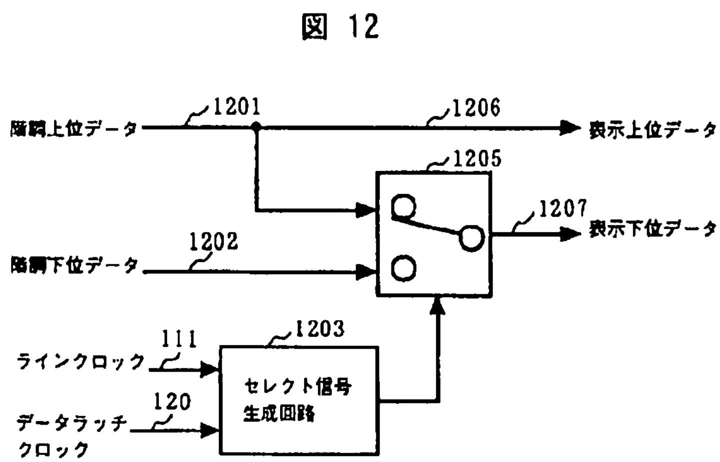


【図11】

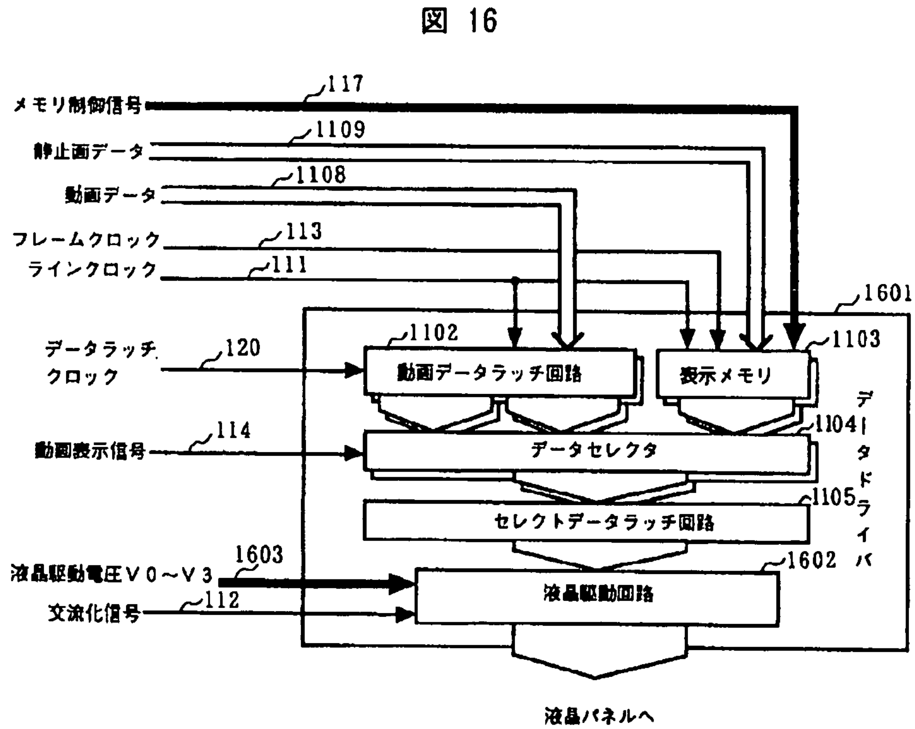
図 11



【図12】



【図16】



フロントページの続き

(72)発明者　古橋　勉
神奈川県川崎市麻生区王禅寺1099番地株式会社日立製作所システム開発研究所内

(72)発明者　恒川　悟
東京都小平市上水本町五丁目20番1号株式会社日立製作所半導体事業部内

(72)発明者　二見　利男
千葉県茂原市早野3300番地株式会社日立製作所電子デバイス事業部内

(72)発明者　西谷　茂之
神奈川県川崎市麻生区王禅寺1099番地株式会社日立製作所システム開発研究所内

(72)発明者　大石　純久
神奈川県川崎市麻生区王禅寺1099番地株式会社日立製作所システム開発研究所内

(72)発明者　犬塚　達裕
神奈川県横浜市戸塚区吉田町292番地株式会社日立画像情報システム内